A T-Shape Connected Multilevel Inverter Topology with a Reduced Number of Switching Devices

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Abstract- This research endeavors a novel configuration for a single-phase Cascaded H-Bridge Multilevel Inverter (CHBMLI) using a stacked T-shape voltage generation module with a view to attaining reduced current conducting switches in the path of load. It involves the use of the collection of a string of voltage generation modules and a two-leg inverter to arrive at a novel Multilevel Inverter (MLI) topology. The MLI permits showcasing the facility of the structural design in an attempt to enlarge the scope of the CHBMLI. It follows a Multicarrier Pulse Width Modulation (MCPWM) approach for synthesizing the Pulse Width Modulation (PWM) output voltage. The prototype augurs the role of a digital PWM controller using Field Programmable Gate Array (FPGA) and the experimental outcomes validate the simulated performance in a wide range of modulation indices. The approach claims a new option of a particular topology for the MLI to suit specific applications in the real world.

Keywords: Multilevel inverter, Multicarrier pulse width modulation, Field programmable gate array, Power switches

1. Introduction

The Multilevel inverters (MLIs) take up a larger consideration in high voltage medium power applications due to their capability of stacking the voltage one over the other in the form of a stepped shape to extract a nearly sinusoidal voltage without the need for filter requirements [1]. There exist several variants in the formation of topologies as reflected in the cascaded inverter [2-3], the neutral point clamped, and the flying capacitor type. The cascade inverter, neutral-point clamped inverter and flying capacitor inverter constitute the basic varieties of MLI topologies [4]. The NPC and FC MLIs require a larger number of clamping diodes and capacitors associated with voltage levels. The cascaded inverter is developed to forfeit its application requirements, the required device count increases significantly high with voltage levels. Multilevel Inverters (MLIs) comprise a group of power semiconductor switches and dc voltage sources to generate stacked voltage waveforms to lease out lower voltage distortion, higher efficiency, reduced switching stress, and lower EMI [4]. The MLI with different voltage sources other than the same voltages owes to the synthesizing of a stacked voltage waveform. The quality of output voltage showcases closer to sinusoidal when the output voltage follows more stepped levels [5-7]. The philosophy engages in pulling out more voltage levels with lesser distortion and assists the use of lower voltage devices. It impinges on its ability to extract waveforms for reaching higher levels of voltages with an improved harmonic spectrum and reduced maximum device rating [8]. The advantages are surmounted to enjoy a lower common-mode voltage, smaller dv/dt, and elimination of low-frequency components in the output voltage. The research perspective exercises the reduced power component topologies that predict lower current conducting switches for a smaller number of power sources to achieve the desired number of levels.

2. Related Work

A new topology for PV applications has been formulated using four switches and a single dc source module, wherein one inductor discharges to tender a boosted voltage at the level of the sub-module. It has been seen to be suitable for PV interfaces, but however, requires a large number of switching components [9]. A hybrid symmetric cascaded topology has been brought out using a 5-level transistor-switched H-bridge and two-leg H-bridge power cells to generate nearly twice the number of output levels as that generated by a conventional symmetric cascaded H-bridge

multi-level converter [10]. It involves a higher number of three level inverters which however tend to increase the total switch count for every added power cell. A single-phase MLI with a flying capacitor on both sides of the H-Bridge inverter has been developed to offer a larger voltage step compared with conventional MLIs. However, the topology has been found to require a capacitor balancing control technique and experiences difficulty in real-time applications [11]. A Z-packed U-cell topology comprising three capacitors and six switching devices has been formed to generate a stepped output voltage [12]. It has been oriented to produce an unbalanced output voltage and needs capacitor voltage balancing. A new series/parallel switched MLI topology has been developed to extradite higher output voltage levels. but the topology has been enticed to operate using switching devices with different blocking voltages [13]. A new MLI topology with high-voltage modules, that includes two dc sources with twice the voltage values as that of the LV module with a single dc source has been presented [14].

A single dc source with multiple series connected H-Bridge inverter along with an isolation transformer has been used to generate a multistep output voltage [15]. It has been projected to use large coupling transformers with an increase in a number of voltage levels. A voltage source inverter (VSI) with K-type dual dc sources and two unequal voltage capacitors has been derived to operate in an un-equal configuration to produce a large number of voltage levels. The modules have been connected in series to synthesize the multilevel output voltage. It has been seen to include a higher number of switching devices with higher voltage blocking capability [16]. A topology based on a transformer coupled with multiple H-Bridge inverters [17], similar to the one cited in [18] has been suggested. A triplet dc source-based configuration with two unidirectional and bidirectional switching devices, suitable for drive applications has been illustrated. It however requires a large number of power components to attain desired voltage level. A single dc source with stacked capacitor cells and a two-level inverter has been used to formulate the MLI topology. The topology has been seen to require a large number of capacitors and capacitor voltage balancing circuits. A new structure using square T-type with four dc sources has been devised to extract multilevel voltage waveforms. The structure has been showcased to claim higher voltage levels with a lower number of power switches [19].

A combination of a half-bridge cell and a two-level inverter has been used to form a new MLI with a reduced number of power components. The topology has been operated using space vector modulation to generate a switching sequence for synthesizing multistep voltage waveform and is seen to be an extension of the traditional three-level inverters [20]. A sequence of dc links acquired from ac supply attached on either side of the H-6 inverter has been enlivened to produce multilevel output voltage [21]. The bidirectional switches on the input side have been seen to produce unbalanced output voltage under faulty conditions. A combination of a T-type neutral-point-clamped inverter and a floating capacitor (FC) H-bridge has been developed for PV applications. The inverter using two low-frequency switches and dc- links are developed to generate a nine-level waveform. A sensorless voltage control has been developed and a PWM controller is used for regulating the full cycle (FC) voltage at one-quarter of the dc source voltage. A cascaded seven-level inverter with a single input source and a switched capacitor have been presented, where the capacitor charging circuit is seen to use only power switches and remain independent of the load conditions. A new MLI based on a cluster of dc sources on either side of the H-6 inverter, similar to the flying capacitor type replacing capacitors with isolated dc sources has been shown [22]. An H-Bridge inverter with two dc sources connected between the center of each leg has been portrayed to offer a higher number of voltage levels, but the topology exhibited to require a larger number of clamping diodes. A generalized topology constituted using an array of dc sources with bidirectional switches and a two-leg inverter has been brought out to achieve a multilevel voltage waveform [23]. It has been seen to require more bidirectional IGBTs. A five-level inverter with coupled inductors has been developed to offer multistep waveform with reduced switching devices. The topology has been restricted to be used in five-level inverter applications [24].

A novel power MLI consisting of packed U cells (PUC), with each U cell including two power switches and one capacitor has been brought out. It has been poised to offer a higher rate of conversion ratio using a lesser number of capacitors and power devices. A topology based on the high-frequency link (HFL) that imbibes only one power supply for the complete multilevel inverter drive, with an inherent voltage regulation of the voltages supplied among the H-bridges has been suggested. It has been seen to allow voltage control with the specified number of levels with a variable voltage characteristic for the dc source [24]. A new MLI that offers larger voltage steps with fewer power semiconductors is developed. It has been seen to consist of series-connected sub-multilevel converters blocks, optimized for various objectives like switches, capacitors, and standing voltage with maximum output voltage steps. Though a large number of topologies keep emerging, still there exists a considerable need to explore newer ones with an emphasis on reducing the number of power components and capacitors.

3. Problem Statement

The main objective is to design a new topology for a single-phase system that allows for smaller power devices in the current conduction path. The proposed structure takes the form of a T shape and utilizes a Field Programmable Gate Array (FPGA) to generate pulses for switch operation. Through hardware measurements, the methodology aims to validate the simulated results and highlights the advantages of achieving a greater number of voltage levels while improving power quality [25].

Figure 1. illustrates a new structure designed for a single-phase MLI, aiming to achieve higher voltage levels with a reduced number of switching devices. The structure consists of a module, as shown in Figure 1, which incorporates four DC sources arranged in a 'T' shape, an array of switching devices, and a two-leg inverter [11]. The module utilizes a single DC source along with a half-bridge cell to generate the minimum voltage level. It is important to ensure that the

complementary switches do not conduct simultaneously to avoid any interloping issues. The H-Bridge inverter in the proposed structure serves to invert the output voltage [12]. To prevent short-circuiting of the voltage sources (V2k, V1k, V3k, and V4k), it is necessary to ensure that the switching pairs (S1k and S3k), (S2k and S3k), (S4k and S5k), and (S5k, S6k, and S7k) do not turn on simultaneously. When the switches (S1k, S3k, and S4k) are switched on, they connect the voltage sources (V1k and V2k) to the load terminals [26]. On the other hand, the switches (S4k, S6k, and S8k) are responsible for producing the zero level in the output voltage. It can be observed that only two switching devices in the T-Module are conducting at any given time, in contrast to the CHBMLI where eight switching devices remain in the conduction path. Figure 2-8 provides a detailed illustration of the operating modes in the level generation section, which generates various levels of the output voltage for a 9-level inverter. It demonstrates that a single 'T' module can produce nine levels in the output voltage using 12 switching devices, whereas the CHBMLI requires 16 switches to achieve the same output voltage level. Therefore, the relationship between voltage levels, semiconductor switches, DC voltage sources, and voltage generation modules (k) can be expressed by Equations (1) to (3).

No. of voltage levels (m) = (8×k) +3 --------- (1)
No. of switches= (8×k) +6 --------- (2)
No. of dc voltage sources= (4×k) +1 --------- (3)

As the proposed topology incorporates both unidirectional and bidirectional devices to generate voltage levels, the bidirectional device can be implemented in either a common-emitter or source configuration using two IGBTs or MOSFETs. When operating the proposed topology in a symmetrical configuration with a voltage source magnitude equal to Vdc, the blocking voltage values of the switches can be determined based on Equations (4) to (7), as shown in Figure 1.

$V_{S1}= V_{S1}'= V_{dc}$ ---------- (4)
$V_{S1k}= V_{S2k}= V_{S3k}= V_{dc}$ ---------- (5)
$V_{S4k}= V_{S5k}= V_{S6k}= (3\times V_{dc})$ ---------- (6)
$V_{S7k}= V_{S8k}= (4\times V_{dc})$ ---------- (7)

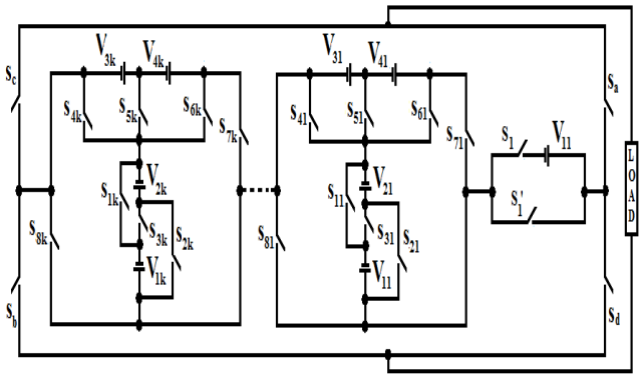

Fig.1. Proposed Topology

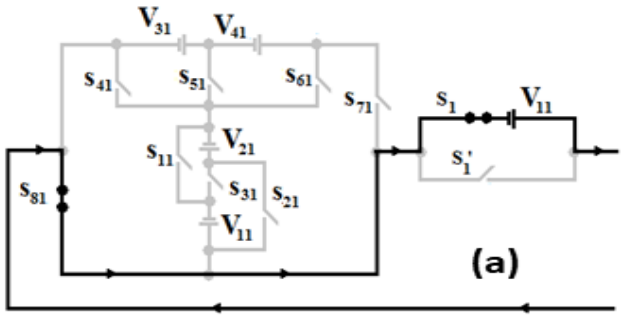

Fig. 3. Operating modes to extract **(a)** $+V_{11}$

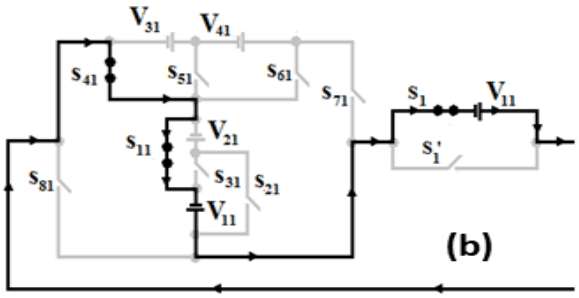

Fig. 4. Operating modes to extract **(b)** + $(V_{11}+V_{11})$

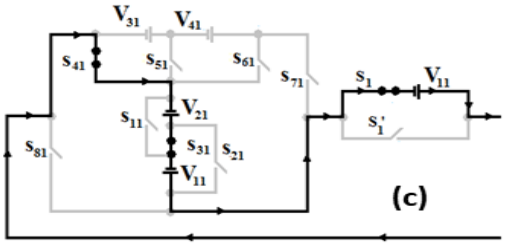

Fig. 5. Operating modes to extract **(c)** $+(V_{11}+V_{11}+V_{12})$

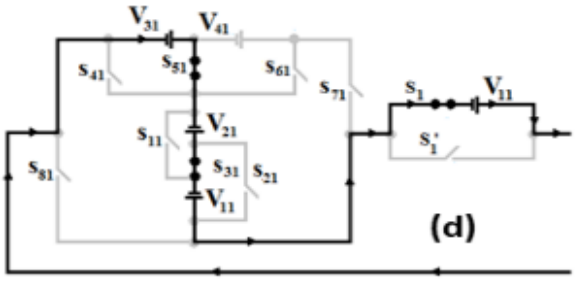

Fig. 6. Operating modes to extract) **d)** + $(V_{11}+V_{11}+V_{12}+V_{13})$

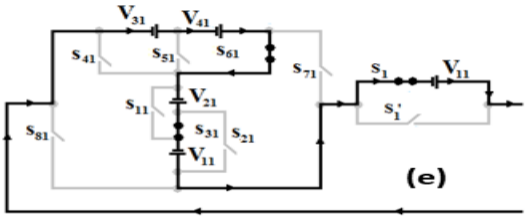

Fig.7. Operating modes to extract **(e)** + $(V_{11}+V_{11}+V_{12}+V_{13}+V_{14})$

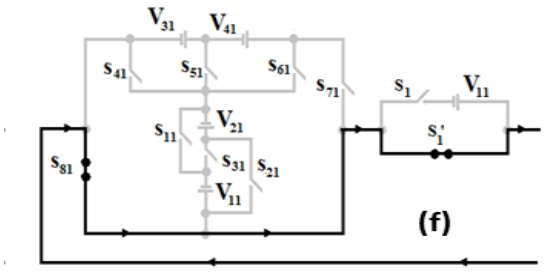

Fig. 8. Operating modes to extract Level Zero

Figures 9 and 10 present a comparison chart illustrating the relationship between the number of switching devices and switches in the conduction path and the number of voltage levels achieved.

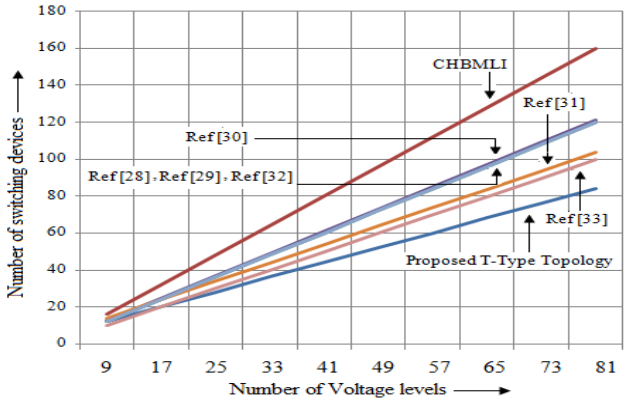

Fig. 9. Variation of switching devices with number of voltage levels

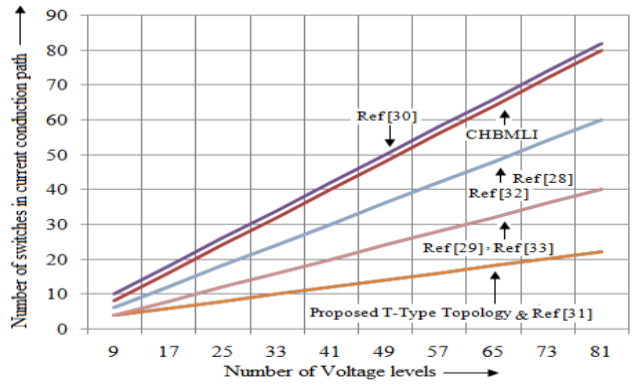

Fig. 10. Variation of switching devices in current conduction path with a number of voltage levels

For instance, in order to achieve a 33-level output voltage, the conventional CHBMLI utilizes 64 switches. On the other hand, the reduced count topologies, as represented, require 48 and 49, 44, and 40 switching devices respectively, while the proposed topology only requires 36 switches to attain the same voltage level [14]. Similarly, when comparing the proposed topology with the CHB and other mentioned topologies, it is evident that the proposed topology involves a reduced number of switches in the conduction path, resulting in a lower total switch count, as shown in Figure 9.The depicted new topology in Figure 10. can be configured in an asymmetrical mode to generate desired voltage levels by adjusting the source voltage magnitudes. Table 1 presents the values of source voltage magnitudes obtained using seven algorithms, showing that the asymmetrical mode produces higher voltage levels compared to the symmetrical mode with the same number of switching devices and voltage sources. The algorithms utilize the T-Type cell as the fundamental block (k) in combination with a half-bridge cell (V1). Pulse Width Modulation (PWM) or fundamental switching can be employed to generate the pulses needed for the desired output voltage level. PWM techniques become more intricate, especially at higher voltage levels, while fundamental switching using the Area Equalization Method (AEM) is applied with the proposed voltage determination algorithms [15]. The PWM can be adjusted to achieve the fundamental switching depicted in Figure 11. using Equations (8 to 12).

$$\propto_j = \sin^{-1}\left(\frac{(2\times j)}{m_a \times (m-1)}\right);\ j = 1,2,3\ldots\left(\frac{m-3}{2}\right) \quad \text{-----} \quad (8)$$

$$\alpha\left(\left(\frac{m-1}{2}\right)^{=\frac{\pi}{2}}\right) \quad \text{---} \quad (9)$$

$$B_1 = \int_{\alpha_{j-1}}^{\alpha_j} (m_a \times \sin \omega i)\, d\,\omega t - \left(\frac{(2\times i)}{(m-1)}\right) \times (\alpha_{i+1} - \alpha_i); i = j-1$$

-------- (10)

Equating the Eqns (3) and (4) to get θ,

$$B_2 = \left(\frac{2}{(m-1)}\right) \times (\alpha_j - \theta_j) \quad \text{------} \quad (11)$$

Equating the Eqns (3) and (4) to get θ,

$$\theta_j = \propto_j - \left(\left(\frac{m_a \times (m-1)}{2}\right) \times \left(cos\,(\alpha_{j-1}) - cos\,(\alpha_j)\right)\right) + \left(i \times (\propto_{i+1} - \alpha_i)\right)$$

---- (12)

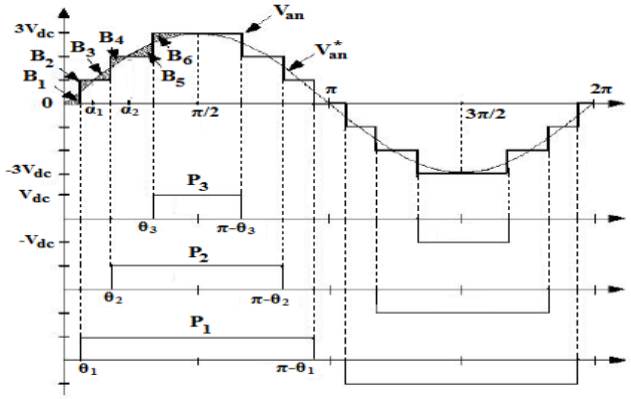

Fig. 11. Conceptual diagram

The modulation index (m_a) and the number of voltage levels (m) are used in the context, where "ma" represents the modulation index, and "m" represents the number of voltage levels [16]. The simulation is conducted in MATLAB, using fundamental switching, with parameters set as k=2, Ma=1, and a maximum output voltage of 300V. Table 2. presents the

switching angles (α1- αn) required to achieve different output voltage levels using equations (8) to (12). Figures 12-17. depict the output voltage and corresponding inductive load current for algorithms (1) to (7). The simulation results demonstrate sinusoidal output voltage waveform, resulting in lower Total Harmonic Distortion (THD) values, as shown in Table 3.

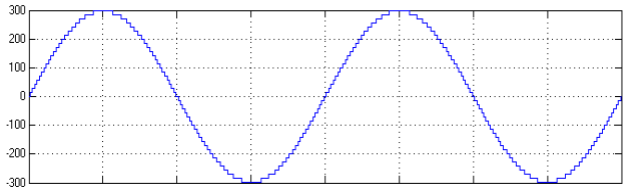

Fig. 12. Y-axis - Output voltage X- axis – time period

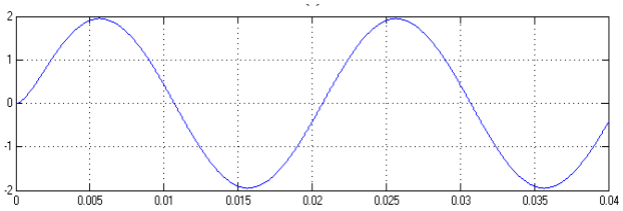

Fig.13. Y-axis - Inductive load current X- axis – time period for 43- level inverter using algorithm-II

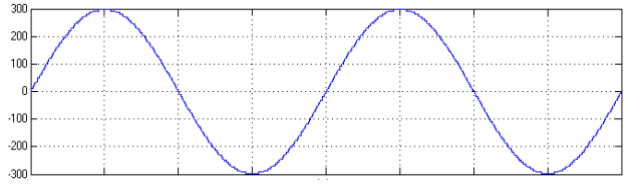

Fig. 14. Y-axis - Output voltage X- axis – time period

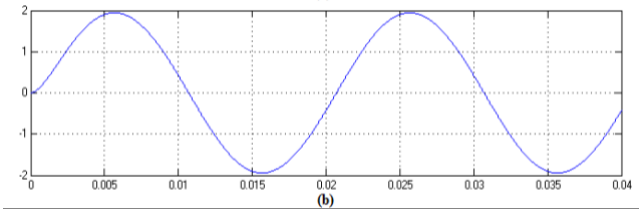

Fig. 15. Y-axis - Inductive load current X- axis – time period for 99- level inverter using algorithm-V

Table 3 indicates that the Total Harmonic Distortion (THD) values decrease as the output voltage levels increase [17]. Among the proposed algorithms, the fifth algorithm exhibits the lowest and progressively decreasing THD values as the voltage level increases with 'k'. Figure 18. illustrates the relationship between the number of T-shaped modules 'k' required to achieve various voltage levels. This prompts a comparison between the proposed algorithms and algorithms associated with recently reduced topologies to assess their respective capabilities in generating different voltage levels [18].

4. Simulation and Experimental results

The effort is to evaluate the performance of the proposed T-Shape topology using MATLAB/Simulink to produce a

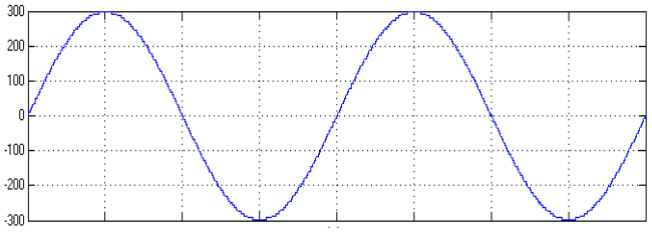

Fig.16. Y-axis - Output voltage X- axis – time period

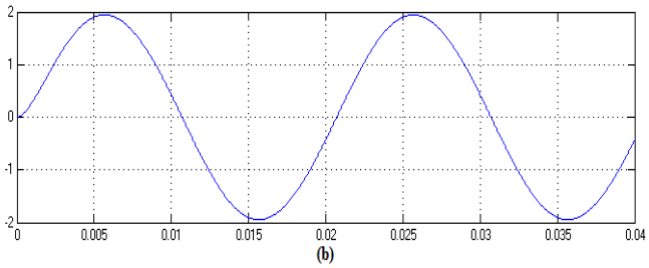

Fig.17. Y-axis - Inductive load current X- axis – time period for 71- level inverter using algorithm-VII

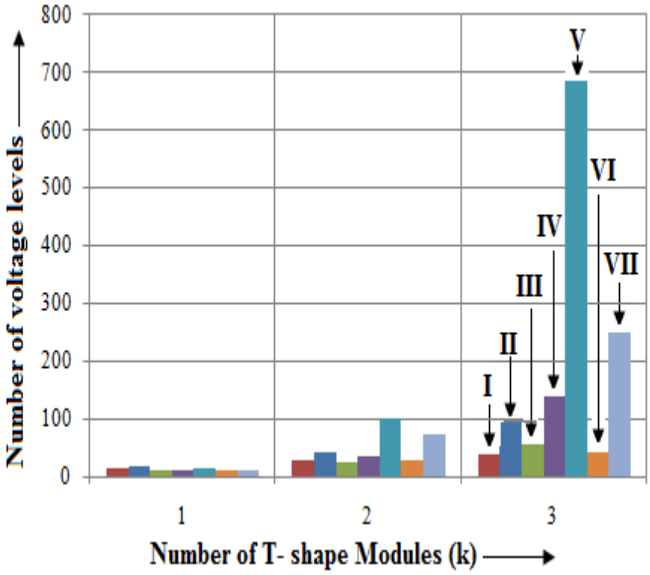

Fig. 18. Variation of 'k' against voltage levels

peak output voltage of 300V (peak) with an RL load of 150Ω and 100mH. It engages the Multicarrier PWM method to generate the PWM pulses for configuring the proposed topology in the symmetrical and asymmetrical modes [19]. It simulates the symmetrical topology for 9-level with the peak output voltage of 300V using 75V and 50 Vdc supply at a switching and reference frequency of 2 kHz and 50 Hz respectively. While the Figure 19. displays the output voltage along with the inductive load current waveform for the symmetric 9- 9-level inverter, Figure 20. shows the output voltage and inductive load current for an asymmetric 15-level inverter [20]. The exercise extends to constitute an experimental prototype using MoSFETS 740 series and 6N137 opto-coupler-based driver circuit and involves the Xilinx Spartan 3E-500 FG320 FPGA controller for generating the gating pulses required for both the

symmetrical and asymmetrical modes. Since the gating pulses obtained from the FPGA controller correspond to 3.3V, it appears to be insufficient for driving the MOSFET modules [21]. Therefore it necessitates the use of the driver units to pull up the FPGA pulses to +12V at the MoSFETs gate terminals

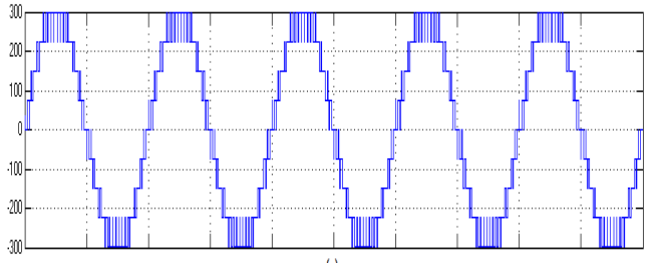

Fig.19. Output voltage

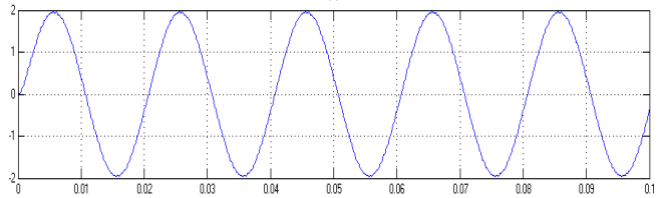

Fig.20. Inductive load current for asymmetrical topology

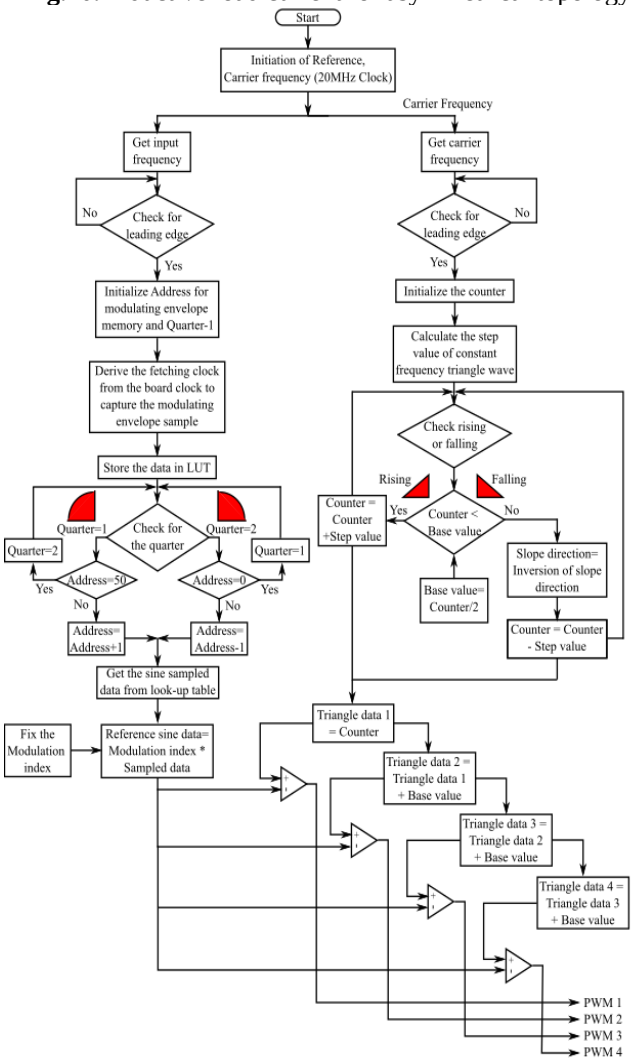

Fig. 21. A flow diagram illustrating the pulse generation methodology using FPGA

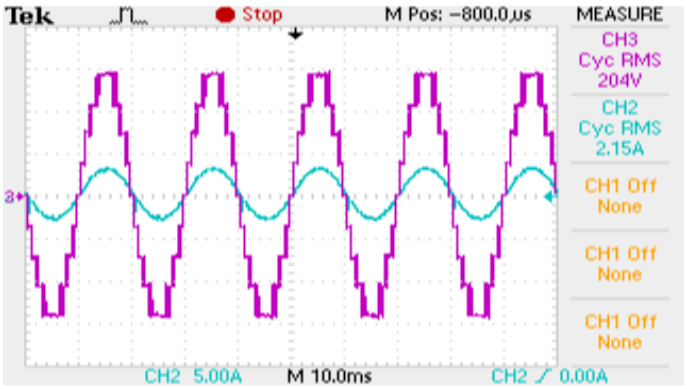

Fig. 22. Combined Output voltage and inductive load current

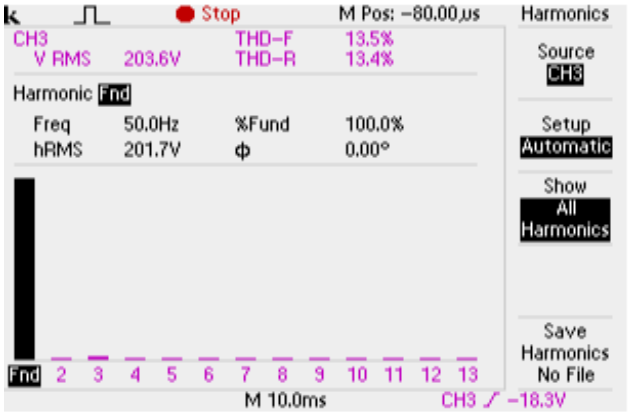

Fig. 23. Voltage spectrum for symmetrical topology

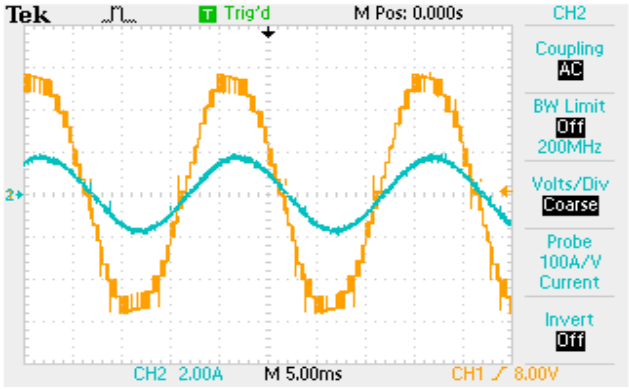

Fig. 24. Combined Output voltage and inductive load current

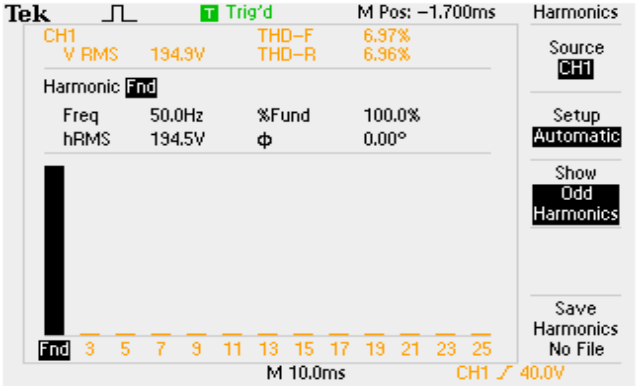

Fig. 25. Voltage spectrum for asymmetrical mode

Figure 21. presents a flow diagram illustrating the pulse generation methodology using FPGA for the Multicarrier PWM (MCPWM) technique [22-25]. The diagram also shows the output voltage, inductive load current, and voltage spectrum for the 9-level inverter, as depicted in Figure 22-25 displays the combined output voltage with inductive load current and harmonic spectrum for the 15-level asymmetrical topology, achieving a peak output voltage of 240V [26-28]. The experimental results shown in both figures serve as validation for the corresponding simulated responses [29-31].

5. Conclusions

Inverters that can operate in both symmetrical and asymmetrical modes have been developed using a novel multilevel inverter topology. The new topology is characterized by reduced switching devices, separate DC input sources, and increased output voltage levels, which offer several advantages over traditional and recently developed topologies. A cascaded topology can be generated by employing seven different methods to determine the magnitude of voltage sources. The algorithms have been demonstrated to achieve nine-level and fifteen-level operating modes through simulation and experiment. The performance and efficiency of the proposed topology are validated by the obtained results. As an interface for renewable energy applications, the proposed MLI topology shows promise. In addition to reducing switching devices, it significantly increases voltage levels while using fewer switching devices. In addition, the high voltage levels and efficient voltage conversion make it suitable for integration with renewable energy sources. The proposed topology uses isolated DC sources and no charging issues are observed in the voltage sources. The proposed topology is suitable for PV applications and the isolated voltage sources are replaced by PV sources. A multilevel voltage generation technology based on the developed MLI topology provides an innovative approach. Various applications, particularly in the renewable energy sector, can be made possible by its superior performance, which has been demonstrated through simulation and experimental results. Power conversion systems can benefit from the reduction of switching devices, the separation of input DC sources, and the increased voltage levels.

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Table 1 Proposed voltage determination algorithms for dc voltage sources in the proposed topology

Proposed algorithms	Values of dc voltage sources	**No. of voltage levels (m)**
I	$V_{1j}= V_{2j}= \mathbf{V_{dc}}$; $V_{3j}= V_{4j}= (\mathbf{2\times V_{dc}})$	$(12\times k)+3$
II	$V_{1j}= \mathbf{V_{dc}}$; $V_{2j}=V_{3j}= V_{4j}= (\mathbf{2^{j}\times V_{dc}})$	$2\times[k+(3\times\sum_{j=1}^{k}2^{j})]+3$
III	$V_{3j}=V_{4j}= \mathbf{V_{dc}}$; $V_{2j}=(\mathbf{3^{j-1}\times V_{dc}})$; $V_{1j}= (\mathbf{2^{j-1}\times V_{dc}})$	$2\times[(2\times k)+(\sum_{j=1}^{k}3^{j-1}+\sum_{j=1}^{k}2^{j-1})]+3$
IV	$V_{1j}= V_{2j}= \mathbf{V_{dc}}$; $V_{3j}=V_{4j}= (\mathbf{5^{j-1}\times V_{dc}})$	$2\times[(2\times k)+(2\times\sum_{j=1}^{k}5^{j-1})]+3$
V	$V_{1j}= V_{2j}=(\mathbf{7^{j-1}\times V_{dc}})$; $V_{3j}= V_{4j}= \mathbf{2\times(7^{j-1}\times V_{dc}})$	$12\times[\sum_{j=1}^{k}7^{j-1}]+3$
VI	$V_{11}= V_{21}= V_{31}= V_{41}= \mathbf{V_{dc}}$; $V_{1j}= V_{2j}= V_{3j}= V_{4j}= (\mathbf{2\times V_{dc}})$	$(16\times k)-5$
VII	$V_{11}= V_{21}= V_{31}= V_{41}= \mathbf{V_{dc}}$; $V_{1j}= (\mathbf{3^{j-1}\times V_{dc}})$; $V_{2j}= V_{3j}= V_{4j}= (\mathbf{3^{j}\times V_{dc}})$	$2\times[4+(3\times\sum_{j=2}^{k}3^{j}+\sum_{j=2}^{k}3^{j-1})]+3$

Table 2 Switching angles obtained using proposed voltage determination algorithms

α (deg)	**I**	**II**	**III**	**IV**	**V**		**VI**	**VII**		**α (deg)**
α_1	2.2048	1.3644	2.3887	1.6857	0.5847	31.3605	2.2048	0.8186	46.7712	α_{26}
α_2	6.6275	4.0964	7.1829	5.0628	1.7543	32.7401	6.6275	2.4564	49.2183	α_{27}
α_3	11.0904	6.8378	12.0284	8.4578	2.9246	34.1415	11.0904	4.0962	51.7933	α_{28}
α_4	15.6228	9.595	16.9633	11.883	4.0961	35.5665	15.6228	5.7394	54.5249	α_{29}
α_5	20.2582	12.3749	22.0321	15.3519	5.2694	37.0174	20.2582	7.3873	57.4536	α_{30}
α_6	25.037	15.1847	27.2905	18.8797	6.4449	38.4965	25.037	9.0414	60.6395	α_{31}
α_7	30.0109	18.0325	32.8123	22.4835	7.6231	40.0066	30.0109	10.7032	64.1793	α_{32}
α_8	35.2494	20.9272	38.704	26.184	8.8045	41.551	35.2494	12.3741	68.2489	α_{33}
α_9	40.8536	23.8791	45.133	30.0064	9.9898	43.1331	40.8536	14.0558	73.2435	α_{34}
α_{10}	46.9835	26.9	52.3996	33.9826	11.1794	44.7574	46.9835	15.7499	80.856	α_{35}
α_{11}	53.9272	30.0042	61.1757	38.155	12.3739	46.4286	53.9272	17.4583	--	α_{36}
α_{12}	62.3302	33.2089	74.3402	42.5825	13.5738	48.1528	62.3302	19.1829	--	α_{37}
α_{13}	74.9595	36.5358	--	47.3516	14.7799	49.9371	74.9595	20.9257	--	α_{38}
α_{14}	--	40.013	--	52.6013	15.9927	51.7901	--	22.689	--	α_{39}
α_{15}	--	43.6777	--	58.5829	17.213	53.7227	--	24.4754	--	α_{40}
α_{16}	--	47.5824	--	65.8615	18.4413	55.7486	--	26.2875	--	α_{41}
α_{17}	--	51.8048	--	76.8596	19.6785	57.8859	--	28.1284	--	α_{42}
α_{18}	--	56.4695	--	--	20.9253	60.1588	--	30.0015	--	α_{43}
α_{19}	--	61.8028	--	--	22.1825	62.6016	--	31.9107	--	α_{44}
α_{20}	--	68.3137	--	--	23.4512	65.2651	--	33.8603	--	α_{45}
α_{21}	--	78.1838	--	--	24.7321	68.2313	--	35.8556	--	α_{46}
α_{22}	--	--	--	--	26.0264	71.6491	--	37.9025	--	α_{47}
α_{23}	--	--	--	--	27.3351	75.8531	--	40.008	--	α_{48}
α_{24}	--	--	--	--	28.6595	82.2751	--	42.1806	--	α_{49}
α_{25}	--	--	--	--	30.0008	--	--	44.4308	--	--

Table 3 Comparison between proposed algorithms in terms of THD at fundamental peak voltage of 300V for k=2

Proposed algorithm	Output voltage level	THD (&)
I	27	3.05
II	43	1.91
III	25	3.30
IV	35	2.35
V	**99**	**0.84**
VI	27	2.35
VII	71	1.16